AFFILIATED INSTITUTIONS

ANNA UNIVERSITY : : CHENNAI 600 025

REGULATIONS - 2009

CURRICULUM II TO IV SEMESTERS (FULL TIME)

M.E. VLSI DESIGN

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	AP9221	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2	VL9221	CAD for VLSI Circuits	3	0	0	3
3	AP9222	Computer Architecture and Parallel Processing	3	0	0	3
4	AP9224	Embedded Systems	3	0	0	3
5	E2	Elective II	3	0	0	3
6	E3	Elective III	3	0	0	3
PRACTICAL						
7	VL9225	VLSI Design Lab II	0	0	4	2
		TOTAL	**18**	**0**	**4**	**20**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	E4	Elective IV	3	0	0	3
2	E5	Elective V	3	0	0	3
3	E6	Elective VI	3	0	0	3
PRACTICAL						
4	VL9234	Project Work (Phase I)	0	0	12	6
		TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICAL						
1	VL9241	Project Work (Phase II)	0	0	24	12
		TOTAL	**0**	**0**	**24**	**12**

TOTAL NO.OF CREDITS TO BE EARNED FOR THE AWARD OF DEGREE
21+20+15+12 =68

LIST OF ELECTIVES
M.E. VLSI DESIGN

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
1	VL9251	Testing of VLSI Circuits	3	0	0	3
2	VL9252	Low Power VLSI Design	3	0	0	3
3	VL9253	VLSI Signal Processing	3	0	0	3
4	VL9254	Analog VLSI Design	3	0	0	3
5	VL9255	Design of Semiconductor Memories	3	0	0	3
6	VL9256	VLSI Technology	3	0	0	3
7	VL9257	Physical Design of VLSI Circuits	3	0	0	3
8	VL9258	Genetic Algorithms and their Applications	3	0	0	3
9	AP9213	Advanced Microprocessors and Microcontrollers	3	0	0	3
10	AP9252	Neural Networks and Its Applications	3	0	0	3
11	VL9261	ASIC Design	3	0	0	3
12	NE9251	Reliability Engineering	3	0	0	3
13	AP9256	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
14	VL9264	Digital Speech Signal Processing	3	0	0	3
15	VL9265	DSP Processor Architecture and programming	3	0	0	3
16	VL9266	Introduction to MEMS System Design	3	0	0	3
17		Special Elective	3	0	0	3

AP9221	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	LT P C 3 0 0 3

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

TOTAL: 45 PERIODS

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, “Analysis and design of Analog IC’s”, Fourth Edition, Willey International, 2002.
2. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company ltd, 2000
3. Nandita Dasgupata, Amitava Dasgupta,”Semiconductor Devices, Modelling and Technology”, Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, “CMOS Analog Circuit Design”, Second Edition-Oxford University Press-2003

VL9221 CAD FOR VLSI CIRCUITS LT P C
3 0 0 3

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley &
2. Sons,2002.
3. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

AP9222 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING LT P C
3 0 0 3

UNIT I THEORY OF PARALLELISM 9

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING 9

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLOGIES 9

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPERSCALAR TECHNOLOGIES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V SOFTWARE AND PARALLEL PROGRAMMING 9

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 PERIODS

REFERENCES:

1. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach" , Pearson Education , 2003.
3. John P.Shen, "Modern processor design . Fundamentals of super scalar processors", Tata McGraw Hill 2003
4. Kai Hwang, "Scalable parallel computing", Tata McGraw Hill 1998.
5. William Stallings, " Computer Organization and Architecture", Macmillan Publishing Company, 1990.
6. M.J. Quinn, " Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen "Parallel Programming", Pearson Education Asia , 2002
8. Harry F. Jordan Gita Alaghband, " Fundamentals of parallel Processing", Pearson Education , 2003
9. Richard Y.Kain, " Advanced computer architecture –A systems Design Approach", PHI, 2003.

AP9224 EMBEDDED SYSTEMS LT P C
3 0 0 3

UNIT I EMBEDDED PROCESSORS 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45 PERIODS

REFERENCES

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.

VL9225	VLSI DESIGN LAB II	LT P C 0 0 4 2

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.

TOTAL: 60 PERIODS

VL9251 TESTING OF VLSI CIRCUITS LT P C
3 0 0 3

UNIT I BASICS OF TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

REFERENCES

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

VL9252 LOW POWER VLSI DESIGN L T P C
3 0 0 3

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation technique – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

REFERENCES

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. Dimitrios Soudris, Christians Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
3. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
5. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.

VL9253 VLSI SIGNAL PROCESSING LT P C
3 0 0 3

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

REFERENCES

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

VL9254 ANALOG VLSI DESIGN LT P C 3 0 0 3

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW- VOLTAGESIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS,Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER- AIDED DESIGN AND ANALOG AND MIXED ANALOG DIGITAL LAYOUT 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 PERIODS

REFERENCES:

1. Mohammed Ismail, Terri Fiez, “Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

VL9255 DESIGN OF SEMICONDUCTOR MEMORIES LT P C 3 0 0 3

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NONVOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

UNIT IV RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT V PACKAGING TECHNOLOGIES 9

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TOTAL: 45 PERIODS

REFERENCES

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3. Betty Prince, “ Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

VL9256 VLSI TECHNOLOGY LT P C
3 0 0 3

UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION 9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL: 45 PERIODS

REFERENCES:

1. S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.
2. Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India. 2003.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000.
4. Wayne Wolf ,"Modern VLSI Design", Prentice Hall India.1998.

VL9257 PHYSICAL DESIGN OF VLSI CIRCUITS LT P C
3 0 0 3

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates,field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic-Ratiocut- partition with capacity and i/o constrants.

Floor planning: Rectangular dual floor planning- hierarchial approach- simulated annealing- Floor plan sizing-

Placement: Cost function- force directed method- placement by simulated annealing-partitioning placement- module placement on a resistive network – regular placement-linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees
Global Routing: Sequential Approaches- hierarchial approaches- multicommodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming
Detailed Routing: Channel Routing- Switch box routing.
Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization

UNIT V SINGLE LAYER ROUTING,CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45 PERIODS

REFERENCES

1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995
2. Preas M. Lorenzatti, “ Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.

VL9258 GENETIC ALGORITHMS AND THEIR APPLICATIONS LT P C 3 0 0 3

UNIT I 9

Introduction,GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT II 9

GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning

UNIT III 9

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT IV 9

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.

UNIT V **9**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45 PERIODS

REFERENCES

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience, 1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.
4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.

AP9213 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS **L T P C 3 0 0 3**

UNIT I MICROPROCESSOR ARCHITECTURE **9**

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM **9**

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM **9**

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor**.**

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS **9**

Instruction set addressing modes – operating modes- Interrupsystem- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER **9**

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers**.**

TOTAL: 45 PERIODS

REFERENCES

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “ , PHI,2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001.

AP9252 NEURAL NETWORKS AND ITS APPLICATIONS L T P C
3 0 0 3

UNIT I BASIC LEARNING ALGORITHMS 9

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feedforward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering - Beamforming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.

UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES: RADIAL BASIS FUNCTION NETWORKS 9

Cover’s Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification.

Support Vector Machines:

Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - $\in$-insensitive Loss Function – Support Vector Machines for Nonlinear Regression

UNIT III COMMITTEE MACHINES 9

Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model

NEURODYNAMICS SYSTEMS

Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems- Lyapunov Stability – Neurodynamical Systems – The Cohen-Grossberg Theorem.

UNIT IV ATTRACTOR NEURAL NETWORKS 9

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications

ADAPTIVE RESONANCE THEORY

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center – Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications

UNIT V SELF ORGANISING MAPS 9

Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications

PULSED NEURON MODELS

Spiking Neuron Model – Integrate-and-Fire Neurons – Conductance Based Models – Computing with Spiking Neurons.

TOTAL: 45 PERIODS

REFERENCES

1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3. Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.
4. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.

VL9261 ASIC DESIGN LT P C
3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 PERIODS

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

NE9251 RELIABILITY ENGINEERING LT P C
3 0 0 3

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliablity of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MAQNAGEMENT 9

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45 PERIODS

REFERENCES

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

AP9256	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	LT P C 3 0 0 3

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 PERIODS

REFERENCES

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.
4. C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

VL9264 DIGITAL SPEECH SIGNAL PROCESSING LT P C
3 0 0 3

UNIT I MECHANICS OF SPEECH 8

Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING 8

Time domain parameters of Speech signal – Methods for extracting the parameters Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function

UNIT III FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING 9

Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder—Channel Vocoder.

HOMOMORPHIC SPEECH ANALYSIS

Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH 10

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

UNIT V APPLICATION OF SPEECH SIGNAL PROCESSING 10

Algorithms: Spectral Estimation, dynamic time warping, hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition –Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification – Voice response system – Speech Synthesis: Text to speech, voice over IP.

TOTAL: 45 PERIODS

REFERENCES

1. Ben Gold and Nelson Morgan, Speech and Audio Signal Processing, John Wiley and Sons Inc. , Singapore, 2004
2. L.R.Rabiner and R.W.Schaffer – Digital Processing of Speech signals – Prentice Hall -1978
3. Quatieri – Discrete-time Speech Signal Processing – Prentice Hall – 2001.
4. J.L.Flanagan – Speech analysis: Synthesis and Perception – 2nd edition – Berlin – 1972
5. I.H.Witten – – Principles of Computer Speech – Academic Press – 1982

VL9265 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING LT P C
3 0 0 3

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR 9

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV ADSP PROCESSORS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED PROCESSORS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio - Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 PERIODS

REFERENCES

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
2. User guides Texas Instrumentation, Analog Devices, Motorola.

VL9266 INTRODUCTION TO MEMS SYSTEM DESIGN LT P C
3 0 0 3

UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN 9

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN 9

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES 9

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

REFERENCES:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.